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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,397	12/12/2003	Wee-Kuan Gan	4413-0132P	9139

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EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,397	GAN ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to: See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 as originally filed on 12/12/2003 are pending in the instant application. Of these, there are 2 independent claims and 3 dependent claims.

Specification

2. The disclosure is objected to because of the following informalities: The disclosure is replete with awkward phrasing which makes the meaning difficult to discern.

a. The last sentence of paragraph 0005 reads "The present invention provides an innovated cost effective a method for reducing the frequency of erasing steps of the flash memory so that the service life of the flash memory can be substantially promoted."

b. Figures 1-10B are identified by roman numerals in addition to figure numbers. Examiner is uncertain as to why the roman numerals are used, and also why the same roman numeral is used with multiple figures.

c. In paragraph 0024, the examiner does not understand the significance of marking the second byte in the redundant page H, and how marking the first and second bytes of the redundant page C and H designates that page 0 of child block 2 belongs to child block 2 as stated in lines 21-22, as it would seem that page 0 is a part of child block 2.

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting

any errors of which applicant may become aware in the specification and ensuring that the invention is clearly explained by the specification.

4. Appropriate correction is required.

Claim Objections

5. **Claim 1** is objected to because of the following informalities: at line 6, the word locating is misspelled. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 1-5** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims use terminology not clearly defined in the specification or known to one of ordinary skill in the art. Some examples of these terms are: "logic page", which the examiner interprets to mean "logical page"; "redundant page", which the examiner interprets as referring to a page that stores metadata for the block; and "check area", which the examiner interprets as being an area in the redundant page containing a specific form of metadata.

8. **Claim 1** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

d. **Claim 1** recites the limitation "the writing method" in line 3. There is insufficient antecedent basis for this limitation in the claim. Claim 1 is directed to a linking method, not a writing method.

e. **Claim 1** recites the limitation "wherein said mother block and said child block are directed at said logic block" in line 7. It is not clear what it means for blocks to be directed at another block. Examiner interprets this limitation to mean that the mother and child blocks have the same logical address.

f. **Claim 1** recites the limitation "said block" in line 9. There is insufficient antecedent basis for this limitation in the claim. Claim 1 refers to multiple blocks. Examiner interprets "said block" to mean "said child block".

g. **Claim 1** recites the limitation "said page" in line 10. There is insufficient antecedent basis for this limitation in the claim. Claim 1 refers to multiple pages. Examiner interprets "said page" to mean "said redundant page".

h. **Claim 1** recites the limitation "recording said page of said child block belonging to a page in said mother block" in line 10. It is unclear if "said page" or "said child block" belong to a page in said mother block, and what it means for a page to belong to another page in a different block.

i. **Claim 1** recites the limitation "using said check area consisting a logic page for identifying whether the data retrieved is from said mother block or child block in the subsequent time." The meaning of this limitation is unclear. Examiner interprets the underlined limitations to mean "consisting of a logical

page", "data to be retrieved is stored in", and "when a subsequent read is performed"

9. **Claim 2** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

j. **Claim 2** recites the limitation "the remaining unmarked pages" in line 17. There is insufficient antecedent basis for this limitation in the claim. Claim 1, on which claim 2 depends, makes no reference to marking or unmarking pages, or the presence of marked or unmarked pages.

10. **Claim 3** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

k. **Claim 3** recites the limitation "Wherein said redundant page in said page of child block is defined as three bytes". A page in a flash memory is a physical region. Examiner interprets this limitation to mean "Wherein said check area in said page of child block is defined as three bytes".

l. **Claim 3** recites the limitation "wherein a first and a second byte represent as pages of said child block". What does it mean for a byte to represent as a block?

11. **Claim 4** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

m. **Claim 4** recites the limitation "said logic area" in line 3. There is insufficient antecedent basis for this limitation in the claim. There is no reference to a logic area in claim 1, but there are references to a logic page, a logic block, and a check area. For the purpose of this examination, Examiner interprets this limitation as referring to the logical page written to the child block.

n. **Claim 4** recites the limitation " said page of said child block " in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. What page of the child block is being referred to?

o. **Claim 4** recites the limitation "the data continuously written into said page of said child block and when said page of child block is full". Examiner interprets this limitation to mean "the data being written to a full page of the child block".

12. **Claim 5** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

p. **Claim 5** recites the limitation "said page" in line 12. There is insufficient antecedent basis for this limitation in the claim. Claim 5 refers to an actual page and a logic page in line 10.

q. **Claim 5** recites the limitation "marking a redundant area of said page in said child block belonging to a page of said mother block". It is unclear what it means for a page in a child block to belong to a page of the mother block.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. **Claims 1,2,4, and 5** are rejected under 35 U.S.C. 102(b) as being anticipated by Pua et al (US 2002/0147882).

15. **Claim 1** is taught by Pua as:

r. *A linking method under a mother and child block architecture for building a check area and a logic page of a child block in a flash memory, wherein when a host writes data into a logic block of said flash memory.* See paragraph 0002, which shows that the current invention is directed to a flash memory device.

s. *The writing method comprising: defining a block corresponding to said logic block as a mother block.* The mother block is defined as the block corresponding to the logical address received from the host in paragraph 0118.

t. *Locating a new block from a backup block and defining said new block as a child block.* See paragraph 0121, which shows that a clean block is taken from the FIFO to create a child block.

u. *Wherein said mother block and said child block are directed at said logic block.* See paragraph 0033, which shows that the mother block and the child block have the same logical address.

v. *Recording the data into a page of said child block.* See paragraph 0124, which discusses step 608 of figure 6, in which the data is written to the child block.

w. *Using a redundant page in said block for creating a check area.* Paragraph 0030 shows that at initialization of the flash memory, all the blocks are searched to determine the relationship between the physical blocks in the flash memory and the logical blocks of the stored data. In order to do this, it is inherent that each block has an area that stores the logical block identifier for the data stored in that physical page. These identifiers form the link table that maps the logical addresses to physical addresses.

x. *Recording said page of said child block belonging to a page in said mother block.* Paragraph 0033 shows that the logical address corresponding to the mother block is mapped to refer to the child block. In order for the memory to be initialized as taught by paragraph 0030, the logical address corresponding to the child block must be recorded in the child block.

y. *And using said check area consisting a logic page for identifying whether the data retrieved is from said mother block or child block in the subsequent time.* As shown in paragraph 0030, at initialization the link table is read from each of the physical blocks of the flash memory. This link table associates a physical block with the corresponding logical block so the system can identify if that logical block should be read from the child physical block or the mother physical block.

16. **Claim 2** is taught by Pua as:

z. *Wherein when a host is ready for reading said page in said logic page, said child block corresponding to said mother block in said logic page is read and the remaining unmarked pages in said child block are read all from said pages of said mother block.* Paragraph 0132 shows that when a read is performed, the logical address sent from the host is converted into the physical address of the block and page. The data is then read from this location, which is the child block.

17. **Claim 4** is taught by Pua as:

aa. *Wherein when said host repeats writing data into said logic area, the data continuously written into said page of said child block and when said page of child block is full, a new block is located for moving a valid block of said mother block and said child block into therein and then said mother block and child block are erased.* In the invention disclosed by Pua, when a write is made to a page that has been written to previously in the child page, a new child is selected in the same manner shown in paragraphs 0118-0130. When a child block is chosen, the mother block is moved into the FIFO queue where it becomes an available block.

18. **Claim 5** is taught by Pua as:

bb. *A linking method under a mother and a child block architecture for building a check area and a logic page of a child block in a flash memory, wherein when a host writes data into a logic block of said flash memory, the writing method*

comprising: See paragraph 0002, which shows that the current invention is directed to a flash memory device.

cc. (a) *Defining an actual page corresponding to a logic page as a mother block.* The mother block is defined as the block corresponding to the logical address received from the host in paragraph 0118.

dd. (b) *Locating a new block and defining it as a child block.* See paragraph 0121, which shows that a clean block is taken from the FIFO to create a child block.

ee. (c) *Writing data into said page of said child block.* See paragraph 0124, which discusses step 608 of figure 6, in which the data is written to the child block.

ff. (d) *Marking a redundant area of said page in said child block belonging to a page of said mother block.* Paragraph 0033 shows that the logical address corresponding to the mother block is mapped to refer to the child block. In order for the memory to be initialized as taught by paragraph 0030, the logical address corresponding to the child block must be recorded in the child block.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jared I Rutz
Examiner
Art Unit 2187

jir

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SUPERVISORY PATENT EXAMINER